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10/042,464

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NXP, B.V.

NXP INTELLECTUAL PROPERTY & LICENSING

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EXAMINER

CHEN, TSE W

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UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE BOARD OF PATENT APPEALS  
AND INTERFERENCES

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*Ex parte* MARTINUS JACOBUS COENEN

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Appeal 2009-002623  
Application 10/042,464  
Technology Center 2100

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Decided: March 15, 2010

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Before JOSEPH L. DIXON, LANCE LEONARD BARRY, and JAY P.  
LUCAS, *Administrative Patent Judges*.

BARRY, *Administrative Patent Judge*.

DECISION ON APPEAL

STATEMENT OF THE CASE

The Patent Examiner rejected claims 1-10. The Appellant appeals therefrom under 35 U.S.C. § 134(a). We have jurisdiction under 35 U.S.C. § 6(b).

#### INVENTION

The Appellant describes the invention at issue on appeal as follows.

The present invention . . . gradually (rather than abruptly) increas[es] the supply current to a digital processing apparatus, in the following manner. A plurality of sub-clocking signals are generated from a master clock signal. The sub-clocking signals change from a power-up rest condition to a continuously free running condition one at a time following an initial switch-on of the digital processing apparatus.

(App. Br. 4.)

#### ILLUSTRATIVE CLAIM

1. A method of power management in a digital processing apparatus, the method comprising: receiving a free-running master clock signal; and generating a plurality of sub-clocking signals from said master clock signal, wherein said plurality of sub-clocking signals change from a power-up rest condition to a continuously free running condition one at a time, following an initial switch-on of said digital processing apparatus (30).<sup>1</sup>

#### PRIOR ART

Smentek

US 5,740,087

Apr. 14, 1998

#### REJECTION

Claims 1-10 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Smentek.

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<sup>1</sup> The claim would be easier to read if a line was skipped between each step of the method as is the common and preferred practice. *See, e.g.*, claim 10 of the applied reference.

### CLAIM GROUPING

Based on the Appellant's arguments, we will decide the appeal of claims 1-10 on the basis of claim 1 alone. *See* 37 C.F.R. § 41.37(c)(1)(vii).

### ISSUE

The Examiner finds "that Smentek does disclose 'continuously free running sub-clock signals generated from a master clock'." (Ans. 6.) The Appellant argues that "[o]nly the two-phase clock CLK, NCLK is continuously free running. Hence, there are no *continuously free running sub-clock signals* generated from a master clock as claimed." (App. Br. 8.) Therefore, the issue before us is whether the Appellant has shown error in the Examiner's finding that Smentek discloses continuously free running sub-clock signals.

### LAW

"It is axiomatic that anticipation of a claim under § 102 can be found only if the prior art reference discloses every element of the claim, and that anticipation is a fact question . . . ." *In re King*, 801 F.2d 1324, 1326 (Fed. Cir. 1986) (citing *Lindemann Maschinenfabrik GMBH v. Am. Hoist & Derrick Co.*, 730 F.2d 1452, 1457 (Fed. Cir. 1984)).

# FINDINGS OF FACT ("FFs")

1. Figure 3 of Smentek follows.

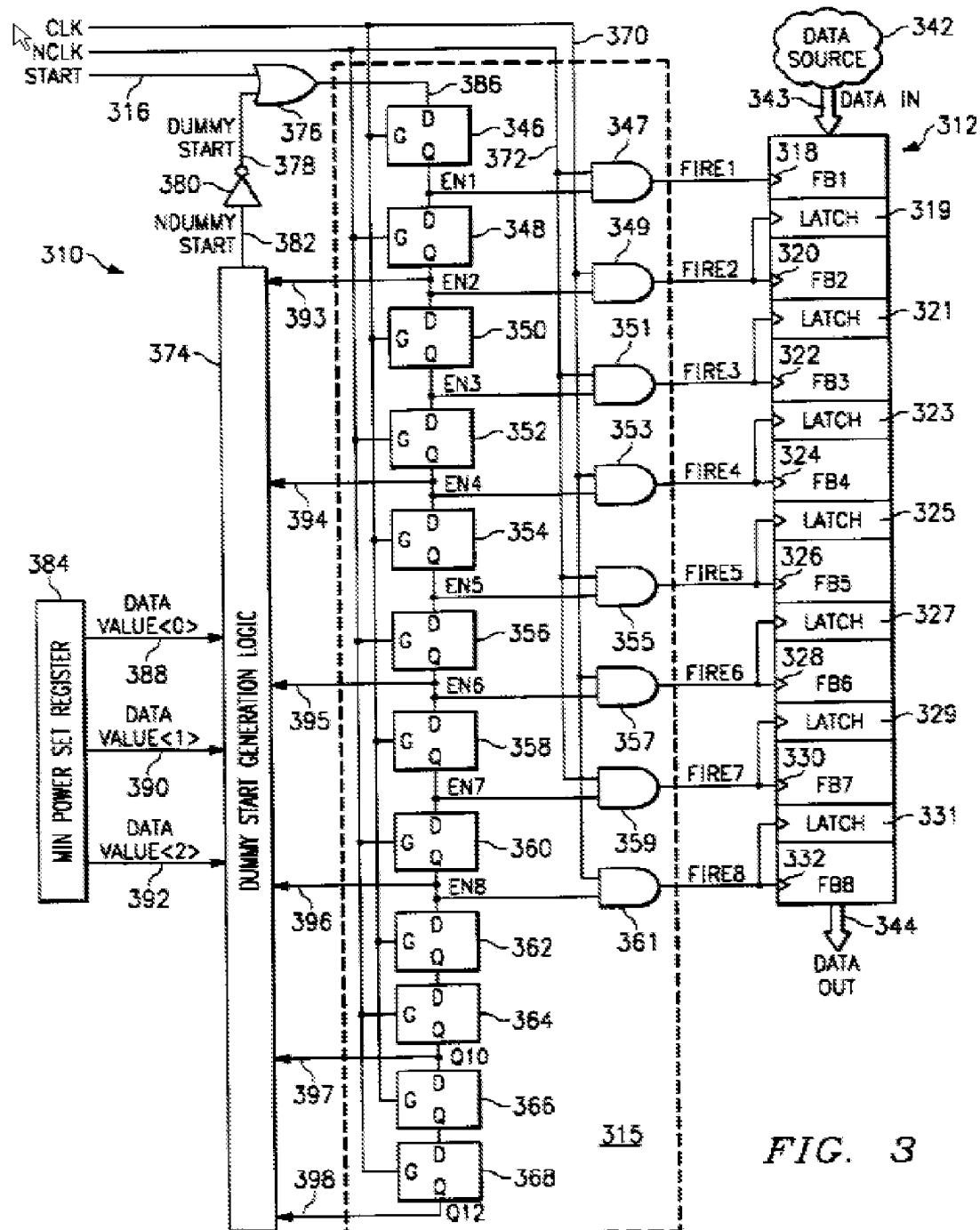


FIG. 3

Figure 3 "is a schematic diagram illustrating an apparatus for regulating power consumption in a digital system 310 . . . ." (Col. 4, ll. 27-29.)

2. The system "compris[es] a pipeline [3]12 of functional blocks FB1-FB8 . . . ." (Col. 2, ll. 66-67.) "[T]he functional blocks are activated by applying a trigger signal, such as 'fire' signals FIRE1-FIRE8, to a trigger input on each functional block, such as trigger inputs [3]18-[3]32." (Col. 3, ll. 4-7.)

3. "A three-bit minimum power set register 384 is also provided." (Col. 4, ll. 48-49.) "The data output of minimum power set register 384 constitutes a data value that corresponds to a desired minimum level of power consumption for pipeline 312 . . . . The data output of minimum power set register 384 is connected to dummy start generation logic 374 . . . ." (*Id.* at ll. 50-56.)

4. "When the data value stored in minimum power set register 384 is 7, then . . . DUMMYSTART will be asserted continuously. Therefore, all of the functional blocks FB1-FB8 in pipeline 312 will be triggered continuously . . . ." (Col. 6, ll. 19-23.)

5. Smentek's "FIG. 1 is a schematic diagram illustrating a prior art digital system comprising a pipeline of functional blocks and a state machine for triggering the functional blocks in sequence responsive to a start signal." (Col. 2, ll. 47-50.) "FIG. 2 is a timing diagram illustrating the operation of the digital system of FIG. 1." (*Id.* at ll. 51-52.)

## ANALYSIS

Smentek discloses an apparatus for regulating power consumption in a digital system. (FF 1.) The system comprises a pipeline 312 of functional blocks FB1-FB8. (FF 2.) The functional blocks are activated by applying trigger signals FIRE1-FIRE8 to trigger inputs 318-332 of functional blocks FB1-FB8, respectively. (*Id.*)

The system also includes a three-bit minimum power set register, the output of which connected to dummy start generation logic. (FF 3.) When a value of 7 is stored in the register, the dummy start generation logic will assert a DUMMYSTART signal continuously. The combination of the DUMMYSTART signal and a master clock ("CLK") signal (*see* Figure 3 of the reference) will continuously trigger all of the functional blocks in the pipeline. (FF 4.) More specifically, the continuous triggering will result from the continuous activation of the fire signal to each functional block. The continuously triggered fires signals constitute continuously free running sub-clock signals.

The Appellant bases his aforementioned argument that there are no continuously free running sub-clock signals generated from a master clock on the premise that "the clock signals EN1-EN8 are generated from the two-phase clock CLK, NCLK on an as-needed basis as seen in Fig. 2. Only the two-phase clock CLK, NCLK is continuously free running." (Appeal Br. 8.) We agree with the Examiner, however, "that the timing diagram shown in figure 2 of Smentek does NOT represent the device of figure 3, but the prior art device of figure 1." (Answer 6.) For its part, the reference

supports the Examiner's position. (*See* FF 5.) The Examiner also finds that "[a]s a matter of fact, Smentek's device of figure 3 is used to solve the problems of prior art figure 1 [col. 1, 11.43-50] by utilizing the DUMMY START signal to provide a continuous free running sub-clock signals for the pipeline stages [i.e., avoid thermal cycling]." (Answer 6.)

The Appellant also argues that "[i]n a pipeline of N stages such as that of Smentek, each stage is clocked at a rate that is 1/N the rate of the master clock. The clocks of the respective stages are therefore, necessarily, gated in a 'one-shot' manner by the state machine 315 of Smentek." (App. Br. 8.) "Argument in the brief does not take the place of evidence in the record." *In re Schulze*, 346 F.2d 600, 602 (CCPA 1965) (citing *In re Cole*, 326 F.2d 769, 773 (CCPA 1964)). Here, the Appellant's argument does not overcome the aforementioned teaching of Smentek that the reference's fires signals are continuously triggered.

#### CONCLUSION

Based on the aforementioned facts and analysis, we conclude that the Appellant has shown no error in the Examiner's finding that Smentek discloses continuously free running sub-clock signals.

#### DECISION

We affirm the rejection of claims 1-10.



Appeal 2009-002623  
Application 10/042,464

No time for taking any action connected with this appeal may be extended under 37 C.F.R. § 1.136(a)(1). *See* 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED

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